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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/740,419	12/19/2000	Andre C. Seznec	1662-25000JMH (POO-3078)	9553

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/740,419	SEZNEC ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22 and 23* is/are allowed.

6)☒ Claim(s) *1-4,6,11-15 and 17* is/are rejected.

7)☒ Claim(s) *5,7-10,16 and 18-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03/04/02* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/20/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-23 are presented for examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4,6,11-15,17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran (5,875,324) in view of Nair et al. (5,890,013).

3. As to claims 1, 11, 12, Tran disclosed a system including at least :

a)a processor (see fig.1);

b) a system memory (fig.1 [system memory]);

c) input device (not explicitly shown);

d) a branch predictor (branch predictor), including a prediction array (see fig.2 [255]) including a single port, that was used for predictions of conditional branches (see col.10, lines 24-40);

e) a multibank control logic coupled the prediction array to ensure that two accesses to the prediction array did not conflict (e.g. see col.189, lines 50-67, col.190, lines 1-29, lines 66-67, col.191, lines 1-4, figs.52,53).

4. Tran did not specifically teach each bank was single ported as claimed. However, Nair disclosed a memory system including a plurality of memory banks,

each was a single-ported bank (e.g. see col.3, lines 39-46). It would have been obvious to one of ordinary skill in the art to use Nair in Tran for including the single ported memory bank as claimed because the sue of Nair could provide Tran the control capability to accept specific access request (such as Read and Write) at a given memory portion based on a predefined sequence of adjusted latency , and therefore, minimizing the circuit space of the memory, and it could be readily achieved by configuring the single-ported memory banks of Nair into Tran with the modified control parameters (e.g. the I/O ports and the port width) so that the single-ported memory banks of Nair could be recognized by Tran, and because Tran also taught the advantage of using a single ported array over the dual ported array (e.g. see col.10, lines 37-40), which was a suggestion of the applicability of the single port into the memory banks as well because one of ordinary skill in the art should be able to recognize the advantage of using a single port of a memory would not be changed regardless of the type of the memory units (e.g. array, bank, cell, segment etc.), and for the above reasons , provided a motivation.

5. As to claims 2,13, Tran also fetched at least two slot of instructions in one cycle (see 32 k bytes of instruction in 16 bytes each fetched in col.5, lines 61-67, col.6, lines 14).

6. As to claims 3,14, Tran also included a multiplexer (e.g. see the selector in col.191, lines 1-10).

7. As to claims 4,15, Tran also determined an index value (e.g. see the index in col.191, lines 1-34).

8. As to claims 6,17, Tran also used 2 bits to be a bank number (see the bits 4:2 selection in col.191, lines 3-5).

9. Claims 5,16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior at of record further teaches the bank identifier for the conditional branch that was different than the bank identifier for a conditional branch that was last used. Tran disclosed bank identifier (banl0-bank7), but it did not teach the determination of the difference of the bank identifier of the last used to access the prediction array.

10. Claims 7-9 , 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the comparison of the two bits value with the last used bank number.

11. Claims 10, 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the pair of the 4-1 mux from the output of the single ported bank. Tran had a multiplexer (selector) , but it was neither a 4-1 mux nor a pair of 4-1 mux.

12. Claims 22,23 are allowable over the art of record. None of the prior art of record teaches the use of the two bits as current bank number if the previous bank

number differs, and the change of the bank number if the previous bank number is equal for a conditional branch to access the prediction array .

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Henry et al. (6,550,004) is cited for the background teaching of the prediction memory array used for conditional branch instructions (e.g. see col.2, lines 40-62).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP